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DESIGN OF 6T AND 8T SRAM CELL WITH MINIMUM EDP- 16NM TECHNOLOGY

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ABSTRACT

Power leakage in a RAM cell is a major concern in today's development of shrinking size and high standby memories. To solve the power leakage problem, many researchers have proposed different ideas from the device level to the architectural level and above. SRAM designs has become the issue of significant research to increase require for laptops, integrated circuit (IC) memory cards, notebooks and hand held communication devices. The work presented here has 6T and 8T SRAM cells, that were designed in S-edit and the simulation is performed using T-spice. The model design of a 6T SRAM cell is traced from the base literature. T-Spice simulation gives the required output by measuring the average power consumed of the MOSFETs along with propagation delay. The simulation is performed using 16nm Technology. The successful operation of the designed cell is verified visually by observing the output waveforms with respect to the input waveforms in W-edit. Upon measuring and performing calculations, it is found that the EDP of 6T Cell in literature was 1.87×10^{20} Ws^2 and as per simulation EDP was 1.26×10^{20} Ws^2. This shows that there is nearly 32.6% increase in power saving upon performing the simulation. Moreover a successful design of 8T SRAM cell is also modeled and the EDP is calculated to be 0.81×10^{-20} against 6T SRAM Cell. This has been achieved by introducing an inverter between BL and BLB.

KEYWORDS: CMOS Logic, Low power, Speed, SRAM and VLSI.

I. INTRODUCTION

The NLP project for Indian Languages is mainly focused on two main tools, i.e. stemmer and lemmatizer. We The SRAM is the most commonly used block in Digital Signal Processing (DSP), therefore its performance and power optimization is of utmost importance for storing the data. With the technology scaling to deep sub-micron, the speed of the circuit increases rapidly. At the same time, the power consumption per chip also increases significantly due to the increasing density of the chip. Therefore, in realizing modern Very Large are one of the basic components in the design of communication circuits. Recently, an overwhelming interest has been seen in the problems of designing digital systems for communication

systems and digital signal processing with low power at no performance penalty. Designing low power high-speed SRAM circuits requires a combination of techniques at four levels; algorithm, architecture, circuit and system levels. They are fast, reliable and efficient components that are utilized to implement any operation. Depending upon the arrangement of the components, there are different types of SRAM available. Particular SRAM architecture is chosen based on the application. The power dissipation in a SRAM is a very important issue as it reflects the total power dissipated by the circuit and hence affects the performance of the device.Very Large Scale Integration (VLSI) includes wadding large number of electronics devices into lesser areas. VLSI is the process of integrating or merging hundreds of thousands of transistors on a single silicon semiconductor microchip. VLSI technology was considered in the late 1970s when advanced level computer processor microchips were under development

II. BASIC ARCHITECTURE AND WORKING OF SRAM

Figure shows the write mode of conventional SRAM cell. Word line is used for enabling the access transistors M1 and M2 for write operation. BL and $\overline{BL}$ lines are used to store the data and its compliment. For write operation one BL is High and the other bit line on low condition.

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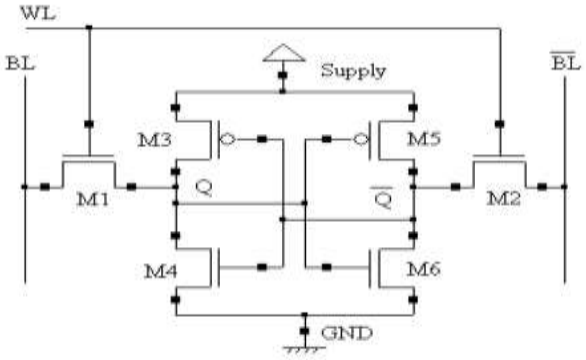

Figure1.1 Conventional 6T SRAM Cell [1]

For writing "0" BL is Low and $\overline{BL}$ is high. When we assert the word line high transistor M1 and M4 is on and any charged stored in the BL goes through M1- M4 path to ground. Due to Zero value at Q the M5 transistor is ON and M6 is OFF so the charged stored at Q. bar line. Similarly in the write "1" operation BL is high due to this M6 is ON and the charge store on is discharged through the M2-M6 path and due to this low value on the M3 is ON and M4 is OFF so the charged stored on the Q.

Memory Architecture is Random-access architecture which is an Asynchronous design. The name is derived from the fact that memory locations (addresses) can be accessed in random order at a fixed rate, independent of physical location, for reading or writing. The storage array, or core, is made up of simple cell circuits arranged to share connections in horizontal rows and vertical columns. The horizontal lines, which are driven only from outside the storage array, are called word lines, while the vertical lines, along which data flow into and out of cells, are called bit lines. A cell is accessed for reading or writing by selecting its row and column. Each Cell can store 0 or 1.

Memories may simultaneously select 4, 8, 16, 32, or 64 columns in one row depending on the application. The row and column (or groups of columns) to be selected are determined by decoding binary address information. For example, consider a row decoder that has 2 n out-put lines, a different one of which is enabled for each different n-bit input code. The column decoder takes m inputs and produces 2 m bit line access signals, of which any of them can be enabled at one time. The bit selection is done using a multiplexer circuit to direct the corresponding cell outputs to data registers. In total, 2 n X 2 m cells are stored in the core array. In this design, the number of rows and columns, both are equal to 64 for 4Mb memory cut.

Using two such memory cuts, a 8Mb SRAM memory is designed. The SRAM IC is R/W memory circuit that permits the modification (writing) of data bits to be stored in a memory array, as well as their retrieval (reading). The SRAM IC was developed using the CDS IC446, cadence IC design environment. The design was based on the AMI 0.6-micron process. The SRAM IC design consists of SRAM cells, pre charge, sense amplifiers, MUX, NAND gates, AND gates, NOR gates and row Decoder. The most important part is the cell as all the other circuitry is connected to and around the cell.

The popular, full CMOS 6-transistor cell configuration was used to design the SRAM memory array. Some of the advantages of using full CMOS SRAM configuration are low static power dissipation, superior noise margins, high switching speeds and suitability for high-density SRAM arrays. In order to design a 64 bit SRAM, 64 full CMOS 6-T cells were used. Each full CMOS 6-T cell has a capability of storing 1 bit.

As per the Literature review we have concluded that there is lot of work done for the reduction of dynamic power dissipation and also there are research paper which is targeting the static power dissipation. As the technology goes down the power dissipation becomes the main design criteria in SRAM memory design. Because memory will decides the total power dissipation. Based on the above literature survey and after carefully analyzing the previous work we have optimized the short circuit power dissipation in SRAM memory cell. Based on the literature survey we have concluded that SRAM memory cell dissipate large amount of short circuit power during rise time and fall time of input data because at that time the direct path exist between the V_{dd} and ground in a single cell the short circuit power is micro watt range at 90 nm technology as the size of

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memory increases the amount of power increases corresponding .so based on the previous work we have decided to optimize the short circuit power.

Static random access memory (SRAM), the most widely used embedded memory, typically occupies the largest portion of SoC die area, and often dominates the total chip power. In order to maintain performance, however, this has required a corresponding reduction in the transistor oxide thickness to provide sufficient current drive at the reduced supply voltages. To further reduce the leakage current, the stacking effect is used by switching off the stack transistors when the memory is ideal**.** The transistors have been lowered which also contributes to leakage currents and reduces the battery life dramatically. The low power reduction techniques reduce the leakage based on the dependencies of the tunneling currents on the terminal voltages, the gate oxide thickness, and the type of the transistor. Various efficient techniques which gives overall best performance over existing SRAM design approaches that allow the analysis and simulations of different parameters at 90nm and 45nm technology successfully on the basis of the power dissipation, speed and their temperature dependence with the area efficiency of the circuit.

III. POWER CONSUMPTION IN CMOS CIRCUITS

There are three main components of power consumption in digital CMOS VLSI circuits.

1) **Switching Power**: consumed in charging and discharging of the circuit capacitances during transistor switching.
2) **Short-Circuit Power**: consumed due to short-circuit current flowing from power supply to ground during transistor switching. This power more dominates in Deep Sub Micron (DSM) technology.
3) **Static Power**: consumed due to static and leakage currents flowing while the circuit is in a stable state. The first two components are referred to as dynamic power, since power is consumed dynamically while the circuit is changing states. Dynamic power accounts for the majority of the total power consumption in digital CMOS VLSI circuits at micron technology [15], [16].

$$P_{avg}=P_{Switching}+P_{Short\text{-}Circuit}+P_{Leakage}$$

$$=(\alpha_{0\rightarrow1}\times C_L\times V_{dd}^2\times f_{clk})+(I_{sc}\times V_{dd})+(I_{leakage}\times V_{dd})$$

Energy Delay Product (EDP)

EDP is a figure of merit that is used in the research. It is basically the product of power consumed with the square of time. Mathematically EDP can be shown as:-

$$EDP = P_{avg} \times (T_{delay})^2$$

This can also be seen as the product of Power Delay with time consumption.

IV. SCHEMATIC OF LOW POWER SRAM CELL

Below Figures are of 1 Bit SRAM Cell using 6T & 8T shows the write mode of low power SRAM cell. Word line is used for enabling the access transistors M1 and M2 for write operation. BL and $\overline{BL}$ lines are used to store the data and its compliment. For write operation one BL is High and the other bit line on low condition. In low power SRAM cell we introduced one Control signal transistor for controlling these transistors. But due to one more transistors area for low power SRAM cell is increased in comparison to Conventional approach. This control transistor uses control select signals which can be properly control the short circuit power dissipation. During write operation this transistor which has control signal works as in on condition. During read operation it will remain in off condition. When this transistor is in off condition will break the path which is in between V_{dd} and Ground

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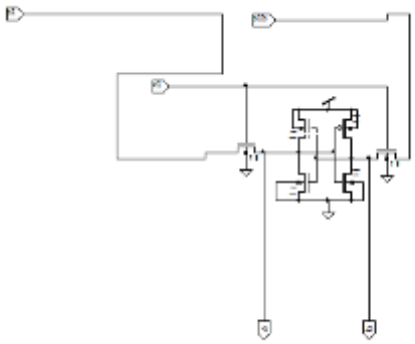


Figure 3.1 6-T SRAM cell

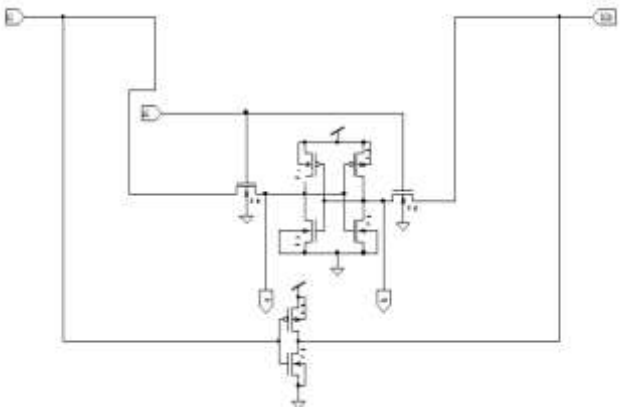
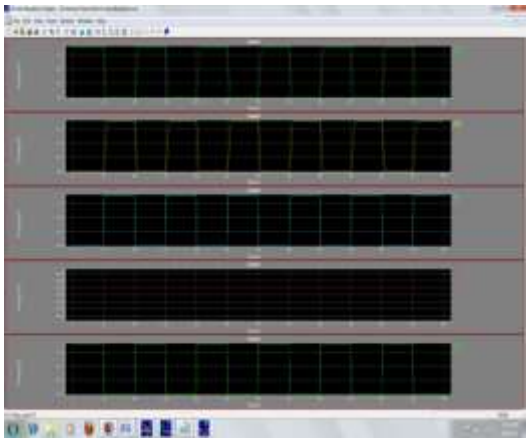


Figure 3.3 8-T SRAM cell

V. FINAL RESULT



Output waveforms of 64-bits SRAM cell

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Performance parameters of Different SRAM Cell

Design Style	Technology Used	Energy Delay Product (Watt Sec^2)	Percentage Improvement
Literature	16nm	1.87×10^{-20}	--------
PRO WORK	16nm	1.26×10^{-20}	32.6%

In above show the output waveforms of 1-bit 6T SRAM cell. The output waveforms of all circuits look like same. But power and delay are the difference between them as shown in below table.

VI. CONCLUSION

The design and implementation of the SRAM memory is shown in this paper. In this paper we design 6T, & 8T SRAM memory cell. The total power consumption is also significantly lower as compared to the existing papers based on SRAM. So according to the requirement we can use these SRAM memory cells can be used in internal CPU. The low power operation is achieved without sacrificing performance of memory. Power consumption is a function of load capacitance, frequency of operation, and supply voltage. A reduction of any one of these is beneficial. A reduction in power consumption provides several benefits. Less heat is generated, which reduces problems associated with high temperature, such as the need for heat sinks. This provides the consumer with a product that costs less. Furthermore, the reliability of the system is increased due to lower-temperature stress gradients on the device. An additional benefit of the reduced power consumption is the extended life of the battery in battery-powered systems. In this paper we concluded that power dissipation and delay are less than the base paper.

VII. APPLICATIONS

SRAMs are basically used as

- Embedded memory, e.g. First and second level caches in processors data buffers in various DSP chips.
- Standalone SRAMs: This can be integrated as an external memory during board design stage.
- Caches in computer systems main memory in low power applications.
- Faster data access speeds.
- Standby power of SRAM memories is very low in spite of high density of transistors.
- SRAM cells have high noise immunity due to larger noise margins, and have ability to operate at lower power supplies.
- Many categories of industrial and scientific subsystems, automotive electronics, and similar, contain static RAM. Some amount (kilobytes or less) is also embedded in practically all modern appliances, toys, etc. that implement an electronic user interface. Several megabytes may be used in complex products such as digital cameras, cell phones, synthesizers, etc.
- SRAM in its dual-ported form is sometimes used for real time digital signal processing circuits.
- SRAM is also used in personal computers, workstations, routers and peripheral equipment internal CPU caches and external burst mode SRAM caches.
- Hard disk buffers, router buffers.
- LCD screens and printers also normally employ static RAM to hold the image displayed Small SRAM buffers are also found in CDROM and CDRW drives usually 256 kb or more are used to buffer track data, which is transferred in blocks instead of as single values. Cable modems and similar equipment connected to computers [2]

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